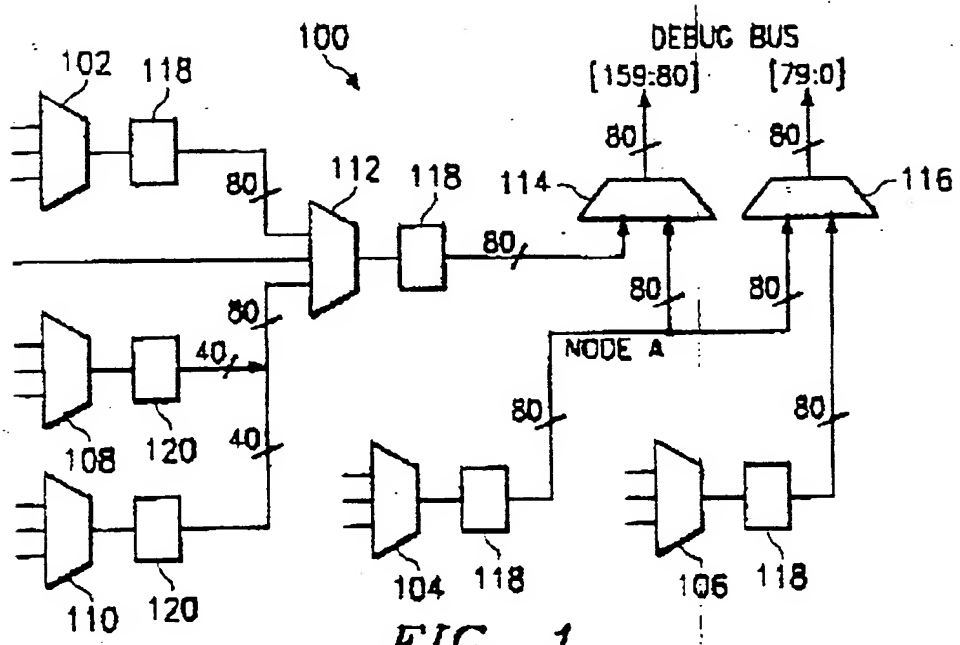
100
DEBUG BUS
[159:80]
[79:0]
102
118
80
112
118
114
116
80
80
80
80
80
NODE A
40
108
120
40
80
80
110
120
104
118
106
118

FIG. 1

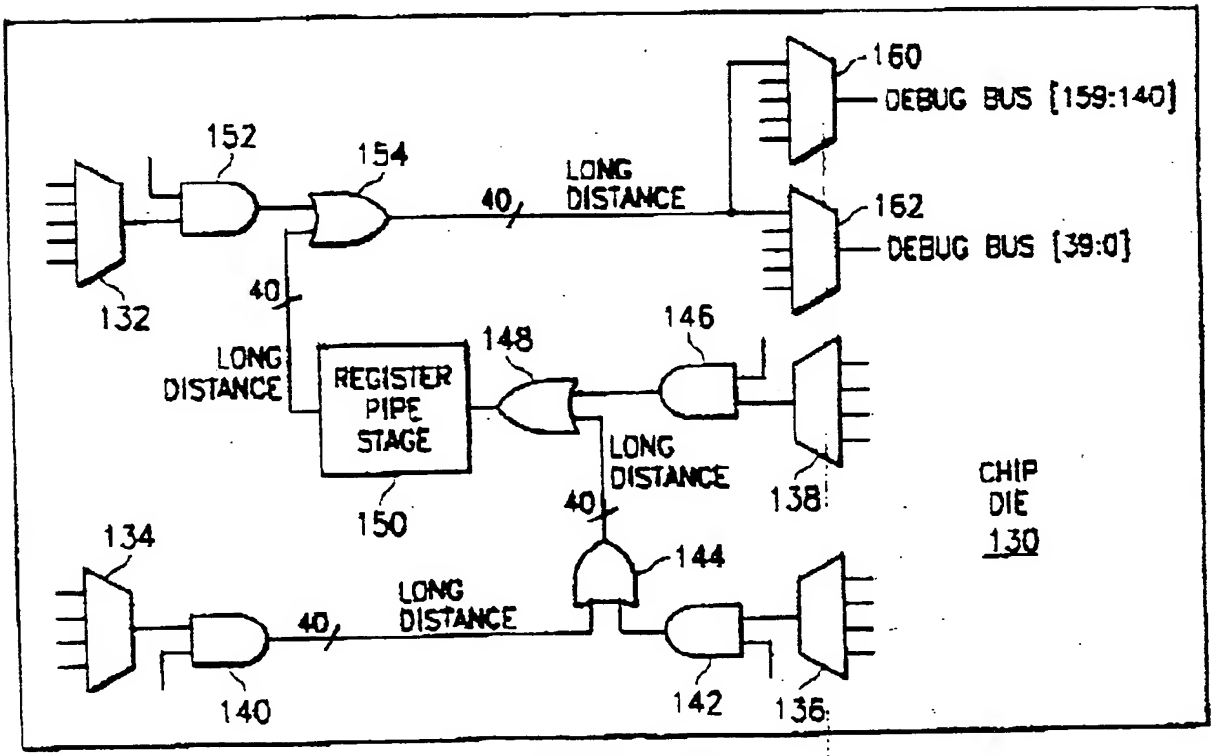
160
DEBUG BUS [159:140]
152
154
LONG
DISTANCE
40
162
DEBUG BUS [39:0]
132
40
LONG
DISTANCE
REGISTER
PIPE
STAGE
148
146
LONG
DISTANCE
138
CHIP
DIE
130
150
40
134
144
LONG
DISTANCE
40
140
142
136

FIG. 2

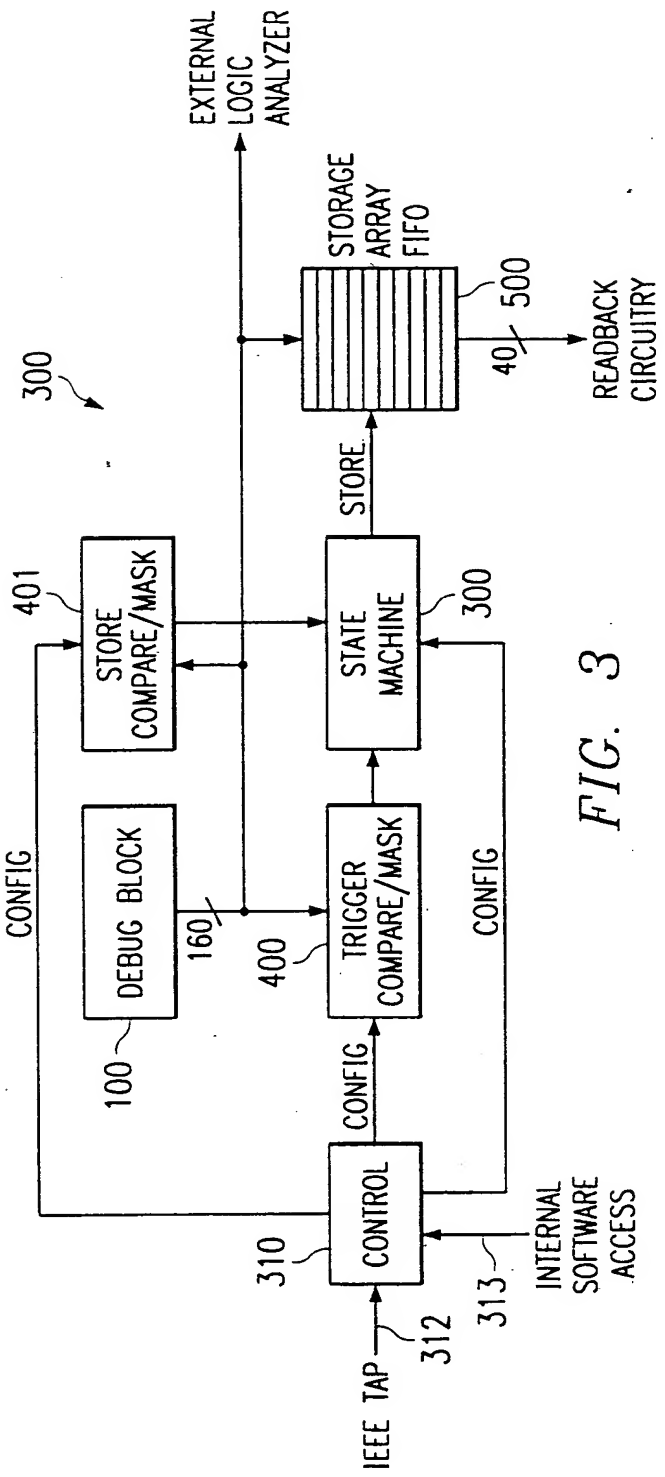
EXTERNAL LOGIC ANALYZER
STORAGE ARRAY FIFO
500
40
READBACK CIRCUITRY
300
STORE
401
STORE COMPARE/MASK
STATE MACHINE
300
CONFIG
DEBUG BLOCK
160
400
TRIGGER COMPARE/MASK
CONFIG
100
CONFIG
310
CONTROL
313
INTERNAL SOFTWARE ACCESS
312
IEEE TAP

FIG. 3

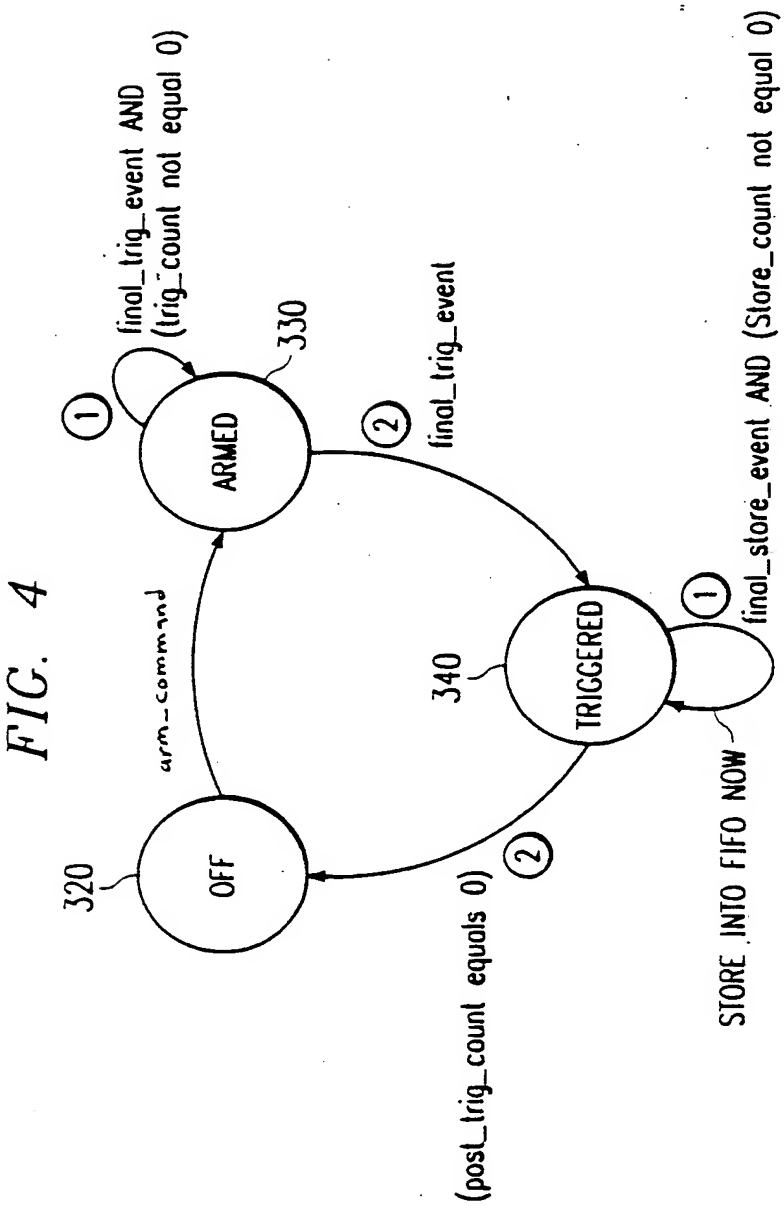
OFF
320
ARMED
330
TRIGGERED
340
arm_command
1
final_trig_event AND
(trig_count not equal 0)
2
final_trig_event
1
final_store_event AND (Store_count not equal 0)
STORE INTO FIFO NOW
2
(post_trig_count equals 0)

FIG. 4

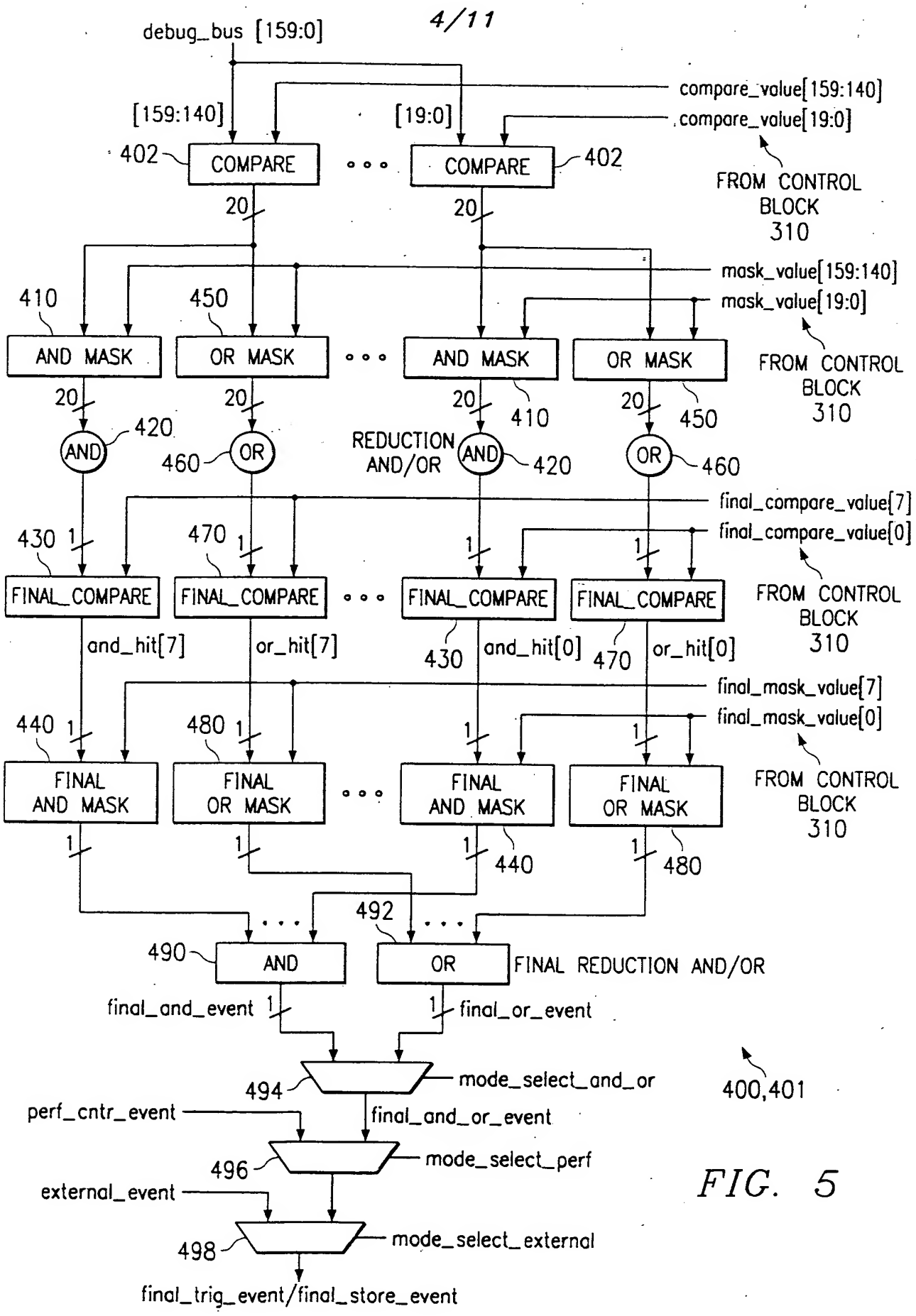
debug_bus [159:0]
[159:140]
[19:0]
compare_value[159:140]
compare_value[19:0]
402
COMPARE
COMPARE
402
FROM CONTROL BLOCK 310
20
20
mask_value[159:140]
mask_value[19:0]
410
450
AND MASK
OR MASK
AND MASK
OR MASK
FROM CONTROL BLOCK 310
20
20
20
410
20
450
AND
420
OR
460
REDUCTION AND/OR
AND
420
OR
460
final_compare_value[7]
final_compare_value[0]
430
1
470
1
1
1
FINAL_COMPARE
FINAL_COMPARE
FINAL_COMPARE
FINAL_COMPARE
FROM CONTROL BLOCK 310
and_hit[7]
or_hit[7]
430
and_hit[0]
470
or_hit[0]
final_mask_value[7]
final_mask_value[0]
440
1
480
1
1
1
FINAL AND MASK
FINAL OR MASK
FINAL AND MASK
FINAL OR MASK
FROM CONTROL BLOCK 310
1
1
1
440
1
480
492
490
AND
OR
FINAL REDUCTION AND/OR
final_and_event
1
1
final_or_event
494
mode_select_and_or
400,401
perf_cntr_event
final_and_or_event
496
mode_select_perf
external_event
498
mode_select_external
final_trig_event/final_store_event

FIG. 5

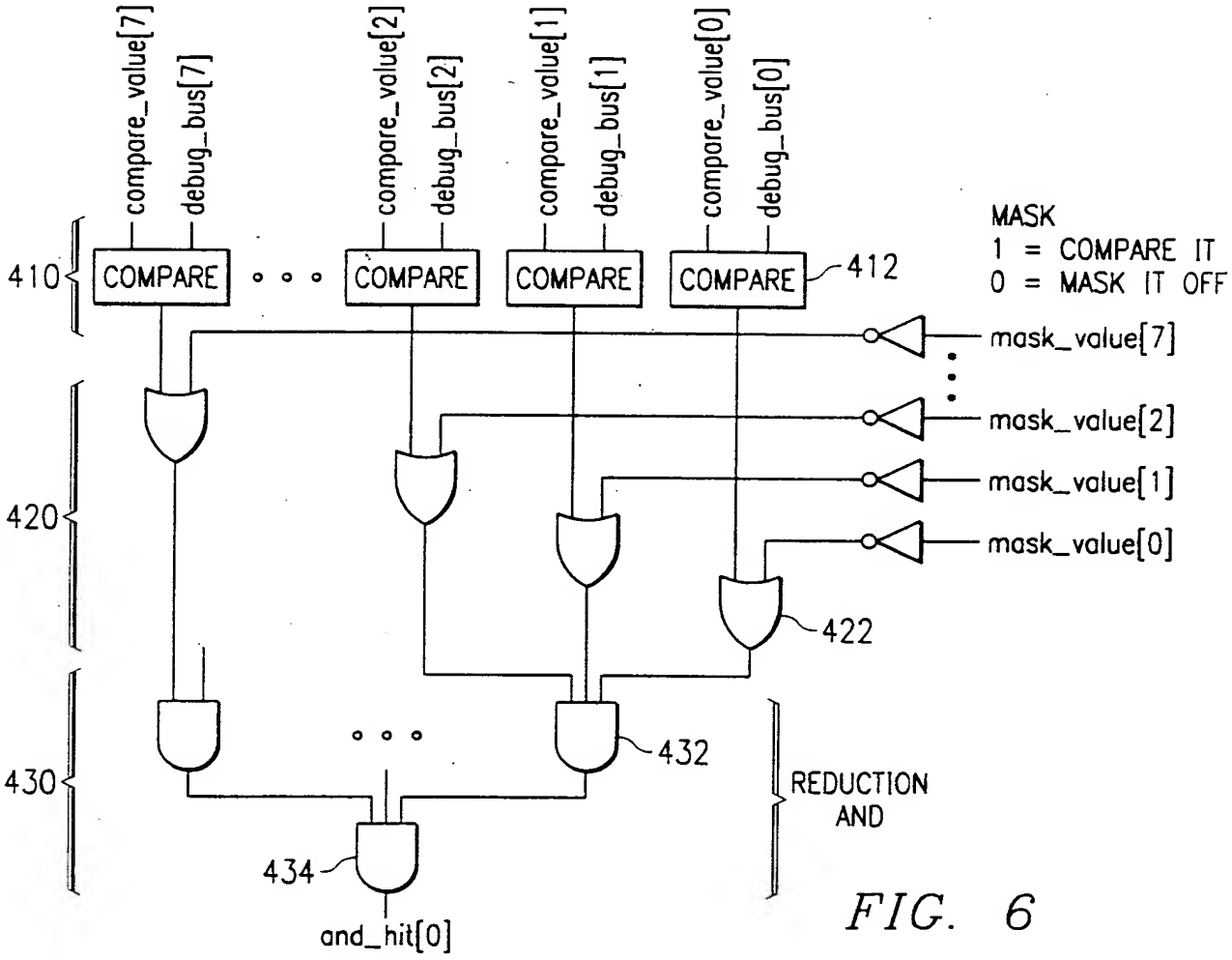
compare_value[7]
debug_bus[7]
compare_value[2]
debug_bus[2]
compare_value[1]
debug_bus[1]
compare_value[0]
debug_bus[0]
MASK
1 = COMPARE IT
0 = MASK IT OFF
410
COMPARE
COMPARE
COMPARE
COMPARE
412
mask_value[7]
mask_value[2]
mask_value[1]
mask_value[0]
420
422
430
432
REDUCTION
AND
434
and_hit[0]

FIG. 6

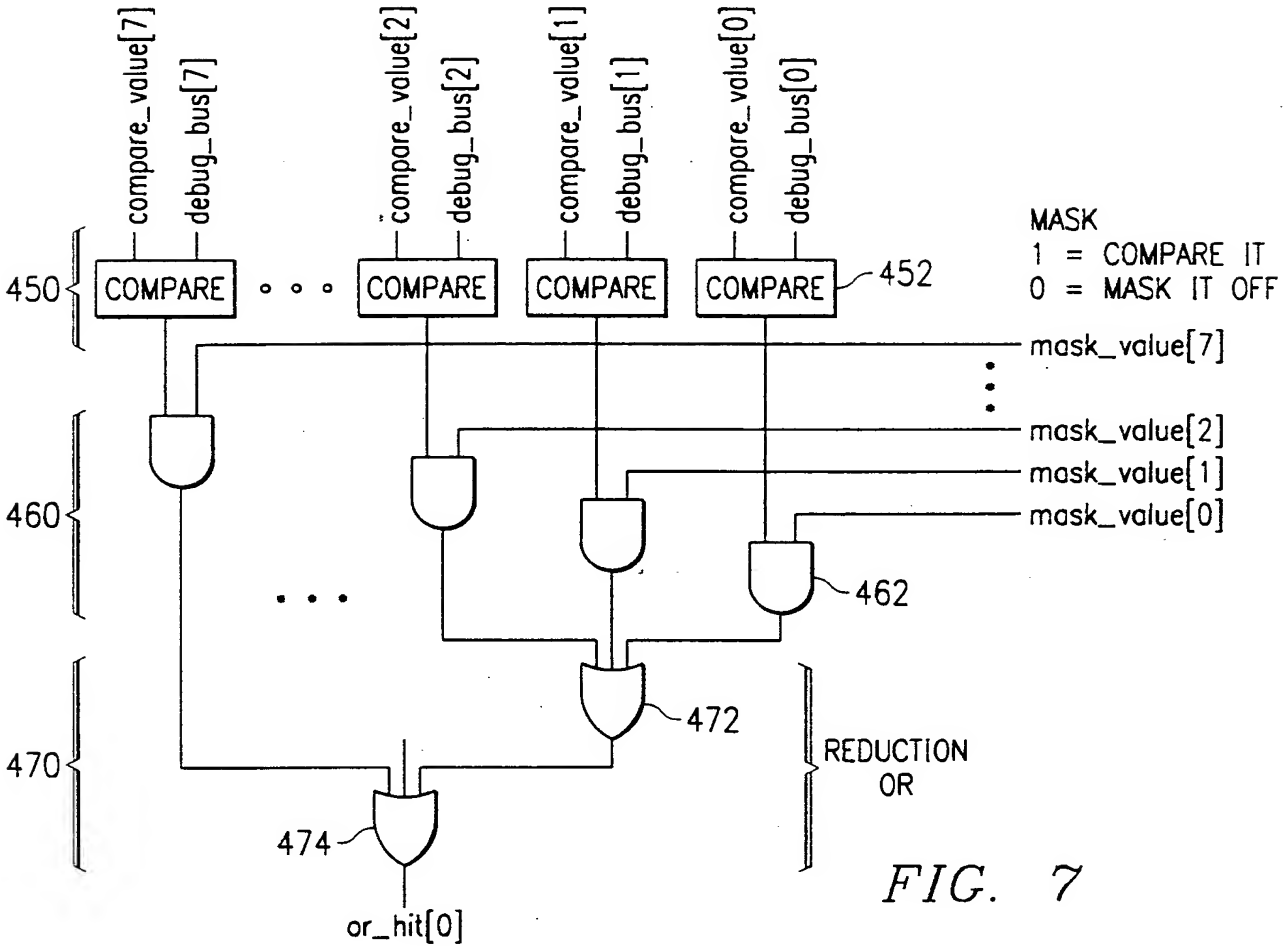
compare_value[7]
debug_bus[7]
compare_value[2]
debug_bus[2]
compare_value[1]
debug_bus[1]
compare_value[0]
debug_bus[0]
MASK
1 = COMPARE IT
0 = MASK IT OFF
450
COMPARE
COMPARE
COMPARE
COMPARE
452
mask_value[7]
mask_value[2]
mask_value[1]
mask_value[0]
460
462
472
470
REDUCTION
OR
474
or_hit[0]

FIG. 7

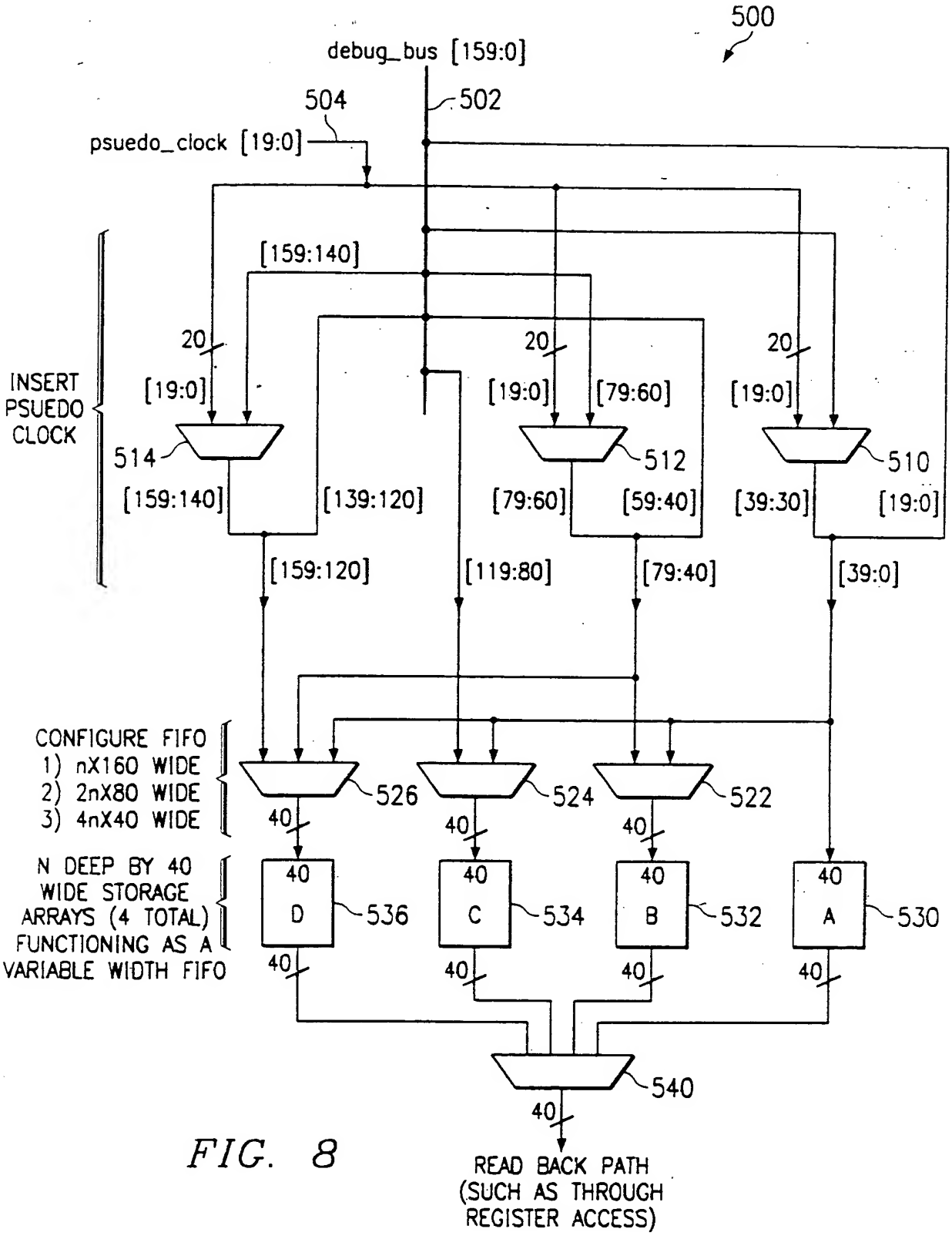
500
debug_bus [159:0]
504
502
psuedo_clock [19:0]
[159:140]
20
20
20
INSERT PSUEDO CLOCK
[19:0]
[19:0]
[79:60]
[19:0]
514
512
510
[159:140]
[139:120]
[79:60]
[59:40]
[39:30]
[19:0]
[159:120]
[119:80]
[79:40]
[39:0]
CONFIGURE FIFO
1) nX160 WIDE
2) 2nX80 WIDE
3) 4nX40 WIDE
526
524
522
40
40
40
N DEEP BY 40 WIDE STORAGE ARRAYS (4 TOTAL) FUNCTIONING AS A VARIABLE WIDTH FIFO
40
D
536
40
C
534
40
B
532
40
A
530
40
40
40
40
540
40
READ BACK PATH (SUCH AS THROUGH REGISTER ACCESS)

FIG. 8

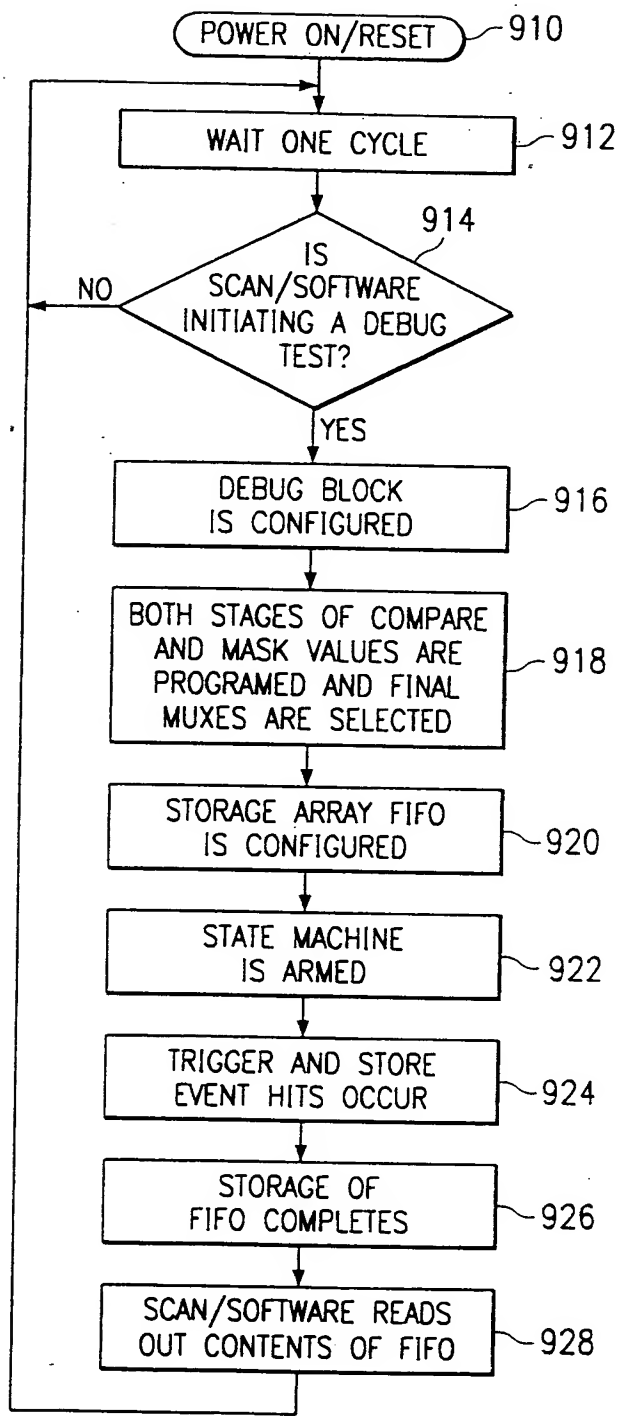
POWER ON/RESET
910
WAIT ONE CYCLE
912
914
IS SCAN/SOFTWARE INITIATING A DEBUG TEST?
NO
YES
DEBUG BLOCK IS CONFIGURED
916
BOTH STAGES OF COMPARE AND MASK VALUES ARE PROGRAMED AND FINAL MUXES ARE SELECTED
918
STORAGE ARRAY FIFO IS CONFIGURED
920
STATE MACHINE IS ARMED
922
TRIGGER AND STORE EVENT HITS OCCUR
924
STORAGE OF FIFO COMPLETES
926
SCAN/SOFTWARE READS OUT CONTENTS OF FIFO
928

FIG. 9

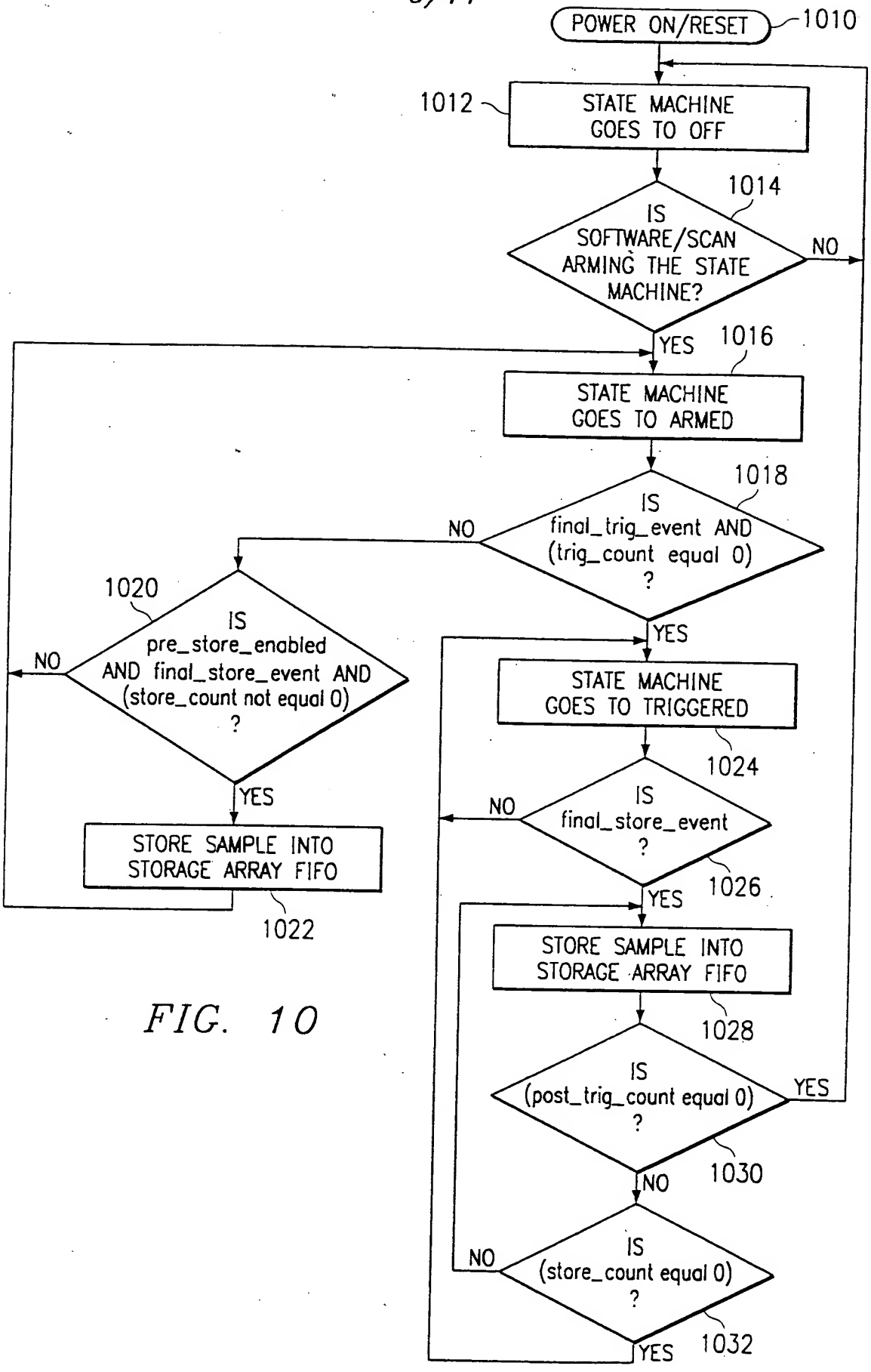
POWER ON/RESET
1010
1012
STATE MACHINE GOES TO OFF
1014
IS SOFTWARE/SCAN ARMING THE STATE MACHINE?
NO
YES
1016
STATE MACHINE GOES TO ARMED
1018
IS final_trig_event AND (trig_count equal 0) ?
NO
YES
1020
IS pre_store_enabled AND final_store_event AND (store_count not equal 0) ?
NO
YES
STORE SAMPLE INTO STORAGE ARRAY FIFO
1022
STATE MACHINE GOES TO TRIGGERED
1024
IS final_store_event ?
NO
YES
1026
STORE SAMPLE INTO STORAGE ARRAY FIFO
1028
IS (post_trig_count equal 0) ?
YES
NO
1030
IS (store_count equal 0) ?
NO
YES
1032

FIG. 10

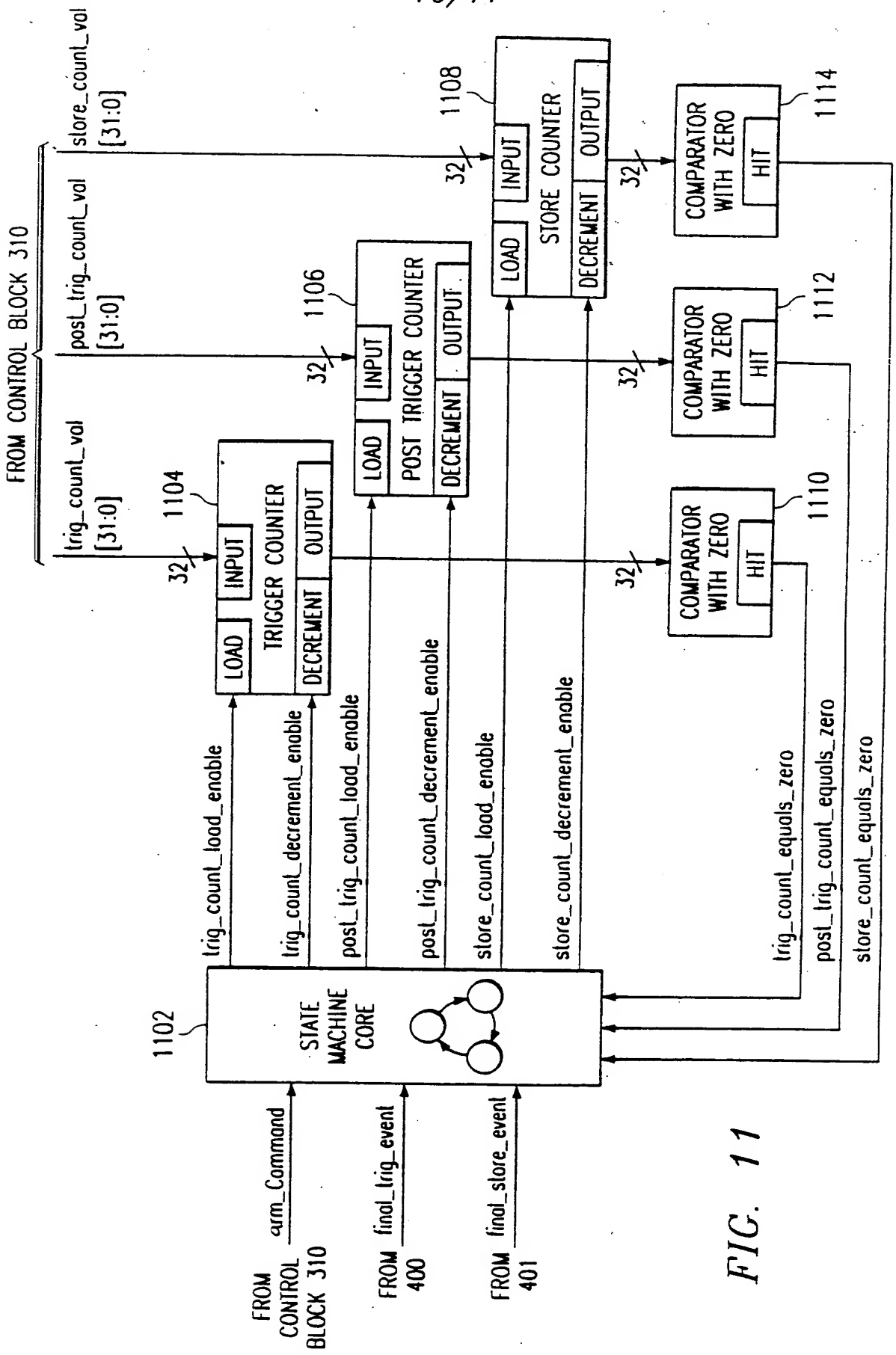
FROM CONTROL BLOCK 310
trig_count_val [31:0]
post_trig_count_val [31:0]
store_count_val [31:0]
1102
STATE MACHINE CORE
1104
TRIGGER COUNTER
LOAD
INPUT
DECREMENT
OUTPUT
1106
POST TRIGGER COUNTER
1108
STORE COUNTER
32
COMPARATOR WITH ZERO
HIT
1110
1112
1114
trig_count_load_enable
trig_count_decrement_enable
post_trig_count_load_enable
post_trig_count_decrement_enable
store_count_load_enable
store_count_decrement_enable
trig_count_equals_zero
post_trig_count_equals_zero
store_count_equals_zero
FROM CONTROL BLOCK 310
arm_Command
FROM 400
final_trig_event
FROM 401
final_store_event

FIG. 11

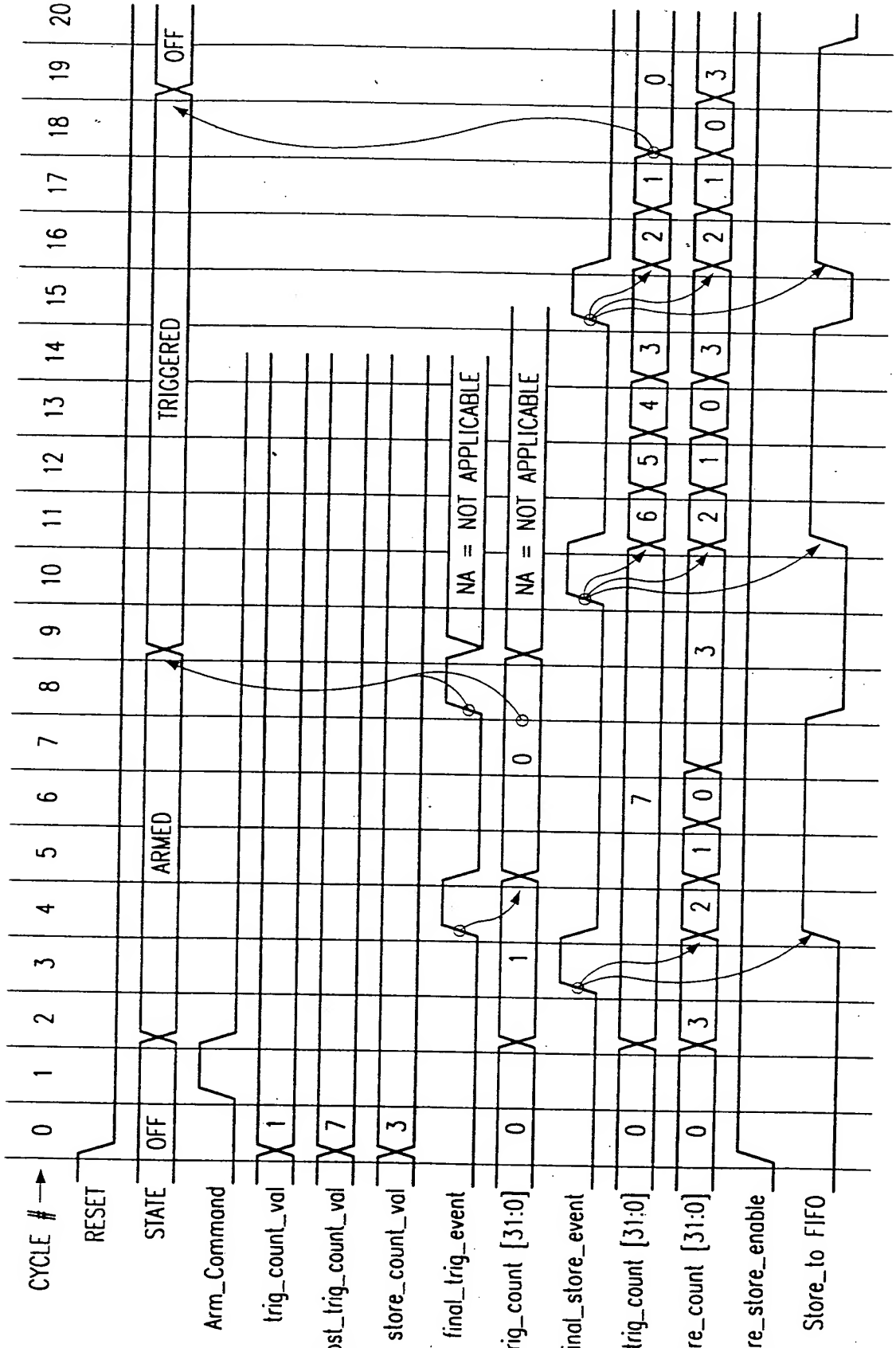
CYCLE #
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
RESET
STATE
OFF
ARMED
TRIGGERED
OFF
Arm_Command
trig_count_val
1
post_trig_count_val
7
store_count_val
3
final_trig_event
trig_count [31:0]
0
1
NA = NOT APPLICABLE
NA = NOT APPLICABLE
0
final_store_event
post_trig_count [31:0]
0
7
6
5
4
3
2
1
0
store_count [31:0]
0
3
2
1
0
3
2
1
0
3
pre_store_enable
Store_to FIFO

FIG. 12